Having described the invention, I claim the following:

1. A pulse width modulator circuit, comprising:

a pulse width driver circuit that receives a time varying ramp signal that is modulated by a time varying analog input signal to produce a pulse width modulated drive signal comprised of turn-on pulses having widths that vary with variations in the magnitude of said input signal;

a switch turned on by each said drive pulse for a time duration dependent upon the duration of each said drive pulse and providing an output signal therefrom;

a negative bias amplifier that provides a negative bias signal that has pulsations that are synchronized with said drive pulses but of opposite phase; and

a combiner that combines said output signal with said bias signal to provide a combined output signal.

2. A modulator circuit as set forth in claim 1 wherein said switch includes a semiconductor switch for

connecting a DC voltage supply source to a load by way of said switch.

3. A modulator circuit as set forth in claim 2 including a filter interconnected between said semiconductor switch and said load.

4. A modulator circuit as set forth in claim 3 including a power amplifier located intermediate said filter and said load and having an output circuit for providing said amplified output signal.

5. A modulator circuit as set forth in claim 4 wherein said output circuit of said power amplifier includes the secondary winding of a first transformer and wherein said negative bias amplifier provides said negative bias output signal at the secondary winding of a second transformer.

6. A modulator circuit as set forth in claim 5 wherein said combiner includes the secondary windings of said first and second transformers with said secondary windings being connected together in series

for providing a summation function to provide said combined output signal.

7. A modulator circuit as set forth in claim 3 including an active load and a second switch for connecting the output of said filter to electrical ground by way of said active load each time a said turn-on drive pulse is provided by said driver circuit.

8. A modulator circuit as set forth in claim 7 wherein a power amplifier located intermediate said filter and said load and having an output circuit for providing said amplified output signal.

9. A modulator circuit as set forth in claim 8 including said output circuit of said power amplifier includes the secondary winding of a first transformer and wherein said negative bias amplifier provides said negative bias output signal at the secondary winding of a second transformer.

10. A modulator circuit as set forth in claim 9 wherein said combiner includes the secondary windings of said first and second transformers with said

secondary windings being connected together in series for providing a summation function to provide said combined output signal.